Closed-Form Bounds for Interconnect-Aware Minimum-Delay Gate Sizing

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Abstract. Early circuit performance estimation and easy-to-apply methods for minimum-delay gate sizing are needed, in order to enhance circuit's performance and to increase designers' productivity. In this paper, we present a practical method to perform gate sizing, taking also into account the contribution of fixed wiring loads. Closed-form bounds are derived and a simple recursive procedure is developed that directly calculate the gate sizes required to achieve minimum delay. The designer, using the proposed method, can easily compare different implementations of the same circuit and explore the energy-delay design space, including in the analysis the effect of interconnect.

1 Introduction

The design of efficient digital circuits requires several decisions that need to be made during the design cycle. One of the major tasks of the designer is to choose the appropriate circuit topology and logic style, determine the sizes of the resulting gates and add extra buffer stages when necessary. Due to the increasing complexity of modern designs and the need for fast and low-power operation, practical and easy-to-apply methods are needed to guide the designer to the best implementation [1]. In this context, the method of Logical effort [2] has been presented that allows the formulation of the gate sizing problem in a simple and comprehensive way.

The problem of sizing simple paths of gates is well understood [3]. However, in almost all cases, simple sizing rules do not suffice, since the effect of intermediate wires should also be taken into account. Handling interconnect effects, when sizing for minimum delay can be performed using sophisticated algorithms or general optimization methods [4]. Such approaches, although solving the sizing problem exactly, do not give the designer the intuition of how the optimal solution was chosen and how performance will change, when choosing another topology or changing the initial placement of the gates in layout. In order the designer to be able to quickly identify which solution matches better the design's constraints, analytical results are needed that would approximate the optimal

* This work has been supported by D. Maritsas Graduate Scholarship of R.A.C.T.I.

V. Paliouras, J. Vounckx, and D. Verkest (Eds.): PATMOS 2005, LNCS 3728, pp. 308–317, 2005.

gate sizes including also the effect of interconnect. In high performance systems, a combined approach is followed. The circuit topology, the number of stages and the logic style are chosen with custom design decisions, while after final placement, a fine tuning step follows that globally optimizes the design for a combined set of constraints [5]–[6]. We limit our discussion to small and medium-sized wires, i.e., wires that scale [7]. Driving longer on-chip wires requires, either the use of repeaters, or the use special signaling techniques [8]. In these cases, the corresponding driver and receiver circuits are designed separately from the modules they connect, and thus, they are not included in the gate sizing procedure.

The problem of analytically approaching the optimal gate sizes, when considering intermediate interconnect capacitances, is considered hard to solve and only a few solutions exist [9]–[10]. However, existing solutions have been derived after making several simplifying assumptions and do not solve the problem in the general case. In this paper, instead of trying to identify an exact solution, we derive closed-form bounds of the gate sizes needed to achieve minimum delay. The proposed bounds are tight enough that allow the approximation of the exact optimal values with almost no loss of accuracy. Also, a simple recursive procedure is developed that solves the problem for paths with multiple levels of intermediate interconnect. The application of the proposed method is straightforward and can help in quickly identifying the optimal number of stages and energy-delay efficient solutions.

The rest of the paper is organized as follows. Section 2 briefly describes the logical effort delay model. Section 3 presents the basic formulation of the proposed approach. In Section 4 the application of the proposed method in selecting the optimal number of stages is described, while in Section 5 a recursive procedure is given that handles gate sizing with multiple levels of interconnect. Finally, conclusions are drawn in Section 6.

2 Gate Delay Model and Simple Path Sizing

Following the logical effort method [2], the delay of a gate is characterized by its output load, its driving capability and its internal parasitic capacitance. These parameters are modelled using the gate's electrical effort $h = C_{\text{out}}/C_{\text{in}}$, its logical effort g, and parasitic delay p, which are combined as $d = \tau(\, g \cdot h + p \,)$. Constant τ is a technology specific parameter that is roughly equal to the delay of unit-sized unloaded inverter. The product of logical and electrical effort $g \cdot h$ is called the stage effort of the gate and it models the delay caused by the gate current charging or discharging the load capacitance. The parasitic delay models the delay needed to charge or discharge the gate's internal parasitic capacitance. The delay model is a first-order approximation of gate's delay yet it is reasonably accurate [11]. In this paper a standard $0.18\mu m$ technology is used for which $\tau \sim 19$ps and 1 FO4 inverter delay is roughly equal to 94ps, under typical conditions and supply voltage of 1.8V.

According to the method of logical effort, a path of N gates achieves minimum delay, when all gates of the path have equal stage effort $f = (G \cdot B \cdot H)^{1/N}$.

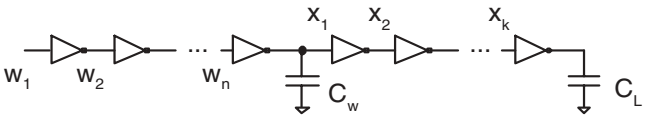


Fig. 1. Two inverter chains separated by fixed wire capacitance C_w

Variables G and B are the product of the logical effort and the branching effort of the gates belonging to the path, and H is the ratio of the final stage loading capacitance to the input capacitance of the first gate of the path. Branching effort b of each gate represents the ratio of all off-path capacitances driven by the gate, to the input capacitance of the following gate of the path.

When fixed off-path wiring capacitances exist in the path, the branching effort of the gate driving the wire cannot be directly estimated [2]. For small wires, the additional off-path loading capacitances can be safely ignored. However, in reality, the floorplan of the circuit imposes the connection of gates that are placed several hundreds of μm apart. Exact analytical gate sizing under this circumstances is efficiently solved by the proposed method.

3 Gate Sizing with Fixed Wiring Capacitance

At first, the proposed methodology will be presented for the case of two inverter chains connected with a wire with capacitance C_w. In the following, the method will be generalized to handle paths of arbitrary logic gates and multiple levels of intermediate interconnect. The two chains of Fig. 1 consist of n inverters with input capacitance w_i, and k inverters with input capacitances x_i, respectively. The load capacitance C_L and the maximum allowed input capacitance w_1 of the first inverter are considered constant. In many practical cases, the value of the loading capacitance and the input capacitance of the path are not known in advance. Therefore the designer should come up with some reasonable numbers. The input capacitance of the first gate is best described by its maximum allowed value. In this case, the inputs of circuit under consideration can be safely driven without slowing down preceding paths.

Following the logical-effort delay model ($g_{inv} = 1$, $p_{inv} = 1.08$), the path delay of the two inverter chains (normalized by τ) is equal to:

$$D = \frac{w_2}{w_1} + \frac{w_3}{w_2} + \cdots + \frac{C_w + x_1}{w_n} + \frac{x_2}{x_1} + \cdots + \frac{C_L}{x_k} + (n+k)p_{inv}$$

Taking the partial derivatives of D with respect to the input capacitances w_i and x_i, and setting them equal to zero, it is derived that the delay is minimized when equations (1) and (2) are satisfied.

$$f_1 = \frac{w_2}{w_1} = \frac{w_3}{w_2} = \cdots = \frac{C_w + x_1}{w_n} \quad \Rightarrow \quad f_1 = \left(\frac{C_w + x_1}{w_1}\right)^{1/n} \tag{1}$$

$$f_2 = \frac{x_1}{w_n} = \frac{x_2}{x_1} = \cdots = \frac{C_L}{x_k} \quad \Rightarrow \quad f_2 = \left(\frac{C_L}{x_1}\right)^{1/k} \tag{2}$$

Variables f_1 and f_2 represent the stage efforts of the first and the second chain of gates, respectively. Due to the fixed wire capacitance, the gates of the two chains when sized for minimum delay need to have unequal stage efforts. The goal is to find f_1 and f_2 that minimize the total path delay, since $D_{\min} = nf_1 + kf_2 + (n+k)p_{inv}$. From (1) and (2) two new equations are derived.

$$f_1^{n-1}\,(f_1 - f_2) = C_w/w_1 \tag{3}$$

$$f_1^{n-1}\,f_2^{k+1} = C_L/w_1 \tag{4}$$

The solution of the two non-linear equations cannot be performed analytically. However we will provide tight bounds on the optimal values of f_1 and f_2 that allow the approximation of the exact values very accurately. Then, the optimal input capacitances could be directly computed from the optimal stage efforts f_1 and f_2 given that $w_i = w_1 \cdot f_1^{i-1}$ and $x_i = C_L/f_2^{k-i+1}$.

3.1 Bounds of Stage Efforts

When the path of Fig. 1 is sized for minimum delay, then according to (3) the optimal value of x_1 is given by the solution of $x_1^{n(k+1)} = w_1^k\, C_L^n\, (C_w + x_1)^{k(n-1)}$. The appropriate value of x_1 strongly depends on the value of C_w. Increasing C_w, also increases the resulting value of x_1. This makes sense since the delay optimization procedure tries to increase the value of x_1 in order to make the effect of the wire capacitance a small fraction of the total. Input capacitance x_1 assumes its minimum nominal value when C_w is equal to zero. Then, both inverter chains form a single path and the problem is treated exactly the same way as in logical effort, briefly described in Section 2. In this case the optimal size of x_1 is $x_{1,\min} = w_1^{k/n+k} \cdot C_L^{n/n+k}$. Based on the definition of stage efforts f_1 (Eq. (1)), for every other non-zero value of the wire capacitance C_w, the value of f_1 should be increased. In this way the last gate of the first chain can better drive both C_w and x_1. Therefore, the value of f_1 should always be greater than $((C_w + x_{1,\min})/w_1)^{1/n}$. Defining X_L and X_W as,

$$X_L = (C_L/w_1)^{n/n+k} \qquad X_W = C_w/w_1 \tag{5}$$

and by replacing the minimum value of x_1, it follows that $f_1 > (\,X_W + X_L\,)^{1/n}$. According to (4), in order the delay to be minimized, every increase in f_1 should be followed by a proportional decrease of the stage effort of the second path. Hence stage effort f_2 is always less than

$$f_2 < X_L^{1/n}\,(\,1 + X_W/X_L\,)^{(1-n)/n(k+1)} \tag{6}$$

We are interested in identifying more tight bounds for the stage efforts f_1 and f_2. Bounding f_1 suffices since the corresponding upper and the lower bounds of f_2 can be easily derived via (4). We will use equations (7) and (8), derived from (3), (4), which express f_1 as a function of f_2 in two different ways.

$$f_1 = \left(\,C_w/w_1 + C_L/(\,w_1 \cdot {f_2}^k\,)\right)^{1/n} \tag{7}$$

$$f_1 = f_2 + (C_w/C_L)\,{f_2}^{k+1} \tag{8}$$

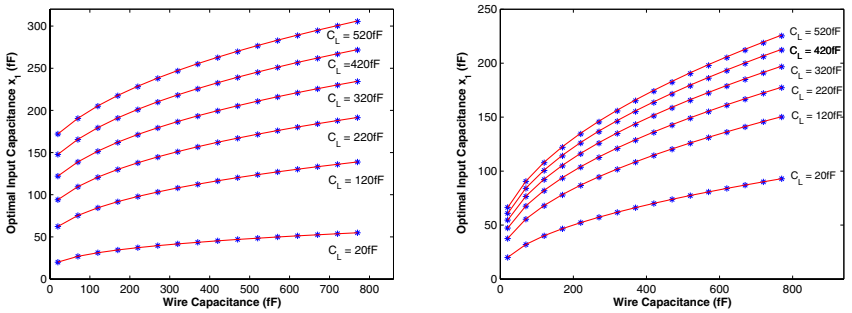


Fig. 2. Optimal and estimated input capacitances of the second chain for various final loads and wire capacitances. The path input capacitance is assumed to be 5fF. (a) The case with three inverters in the first chain and one in the second. (b) The corresponding case with three inverters before and after the wire

Replacing the maximum value of f_2 (Eq. (6)) to (7) and after some algebraic manipulations a tighter lower bound of f_1 can be computed as

$$f_1 > (X_W + X_L \cdot \delta)^{1/n}, \quad \text{where} \quad \delta = (1 + X_W / X_L)^{k(n-1)/n(k+1)} \tag{9}$$

It can be observed that the lower bound of f_1 has the same format as in the case where the wire capacitance is ignored. The only difference is the multiplicative term δ that increases the first lower bound closer to the optimal value. The maximum value of f_1 can be calculated via (9), (4) and (8), and is given by

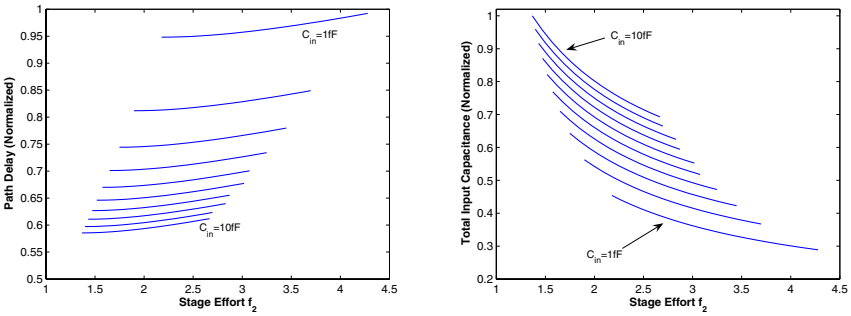
$$f_1 < X_W (X_W + X_L \cdot \delta)^{(1-n)/n} + X_L^{1/n} (\delta + X_W/X_L)^{(1-n)/n(k+1)} \tag{10}$$

The equivalent tight bounds of f_2 are derived by replacing in (4) the minimum and the maximum value of f_1.

$$\left(C_L/(w_1 {f_{1,\min}}^{n-1}) \right)^{1/(k+1)} < f_2 < \left(C_L/(w_1 {f_{1,\max}}^{n-1}) \right)^{1/(k+1)} \tag{11}$$

The proposed bounds of the stage efforts are very tight and the expected values of f_1 and f_2 can be derived by computing the geometric mean of their minimum and maximum value, i.e, the square root of the product of the two extreme points, $f_1^* = \sqrt{f_{1,\min} f_{1,\max}}$. Consider for example the case that $n = 2$, $k = 1$ and $w_1 = 10$fF, $C_w = 50$fF, and $C_L = 100$fF. Solving (3) and (4) numerically it is derived that the minimum value of D is $(8.28 + 3p_{inv})\tau$ and it is achieved when $x_1 = 57.2$fF and the stage efforts f_1 and f_2 are equal to 3.27 and 1.74, respectively. Following the proposed approach, at first we compute $X_L = 10^{2/3} = 4.642$, $X_W = 5$, and $\delta = 1.2$. Then from (9)–(11) the stage efforts f_1 and f_2 are easily bounded to $3.252 < f_1 < 3.291$ and $1.743 < f_2 < 1.754$. Therefore, the expected values of f_1 and f_2 are equal to 3.271 and 1.748, respectively. It is evident that the derived stage efforts and the precomputed values match exactly.

The proposed solution is accurate irrespective of the values of the design parameters. Figure 2 shows the value of the optimal input capacitance x_1 for



(a) (b)

Fig. 3. (a) The delay and (b) the total input capacitance of an example path for various values of stage effort f_2. The path consists of three inverters in the first chain and one in the second. The wire and the loading capacitance are 50 and 100fF, respectively

several configurations, derived both exactly (asterisk points) using MATLAB, and using the proposed bounds (solid line). For both cases the maximum absolute error is less than 0.8fF, which is negligible. Sizing for minimum delay in the presence of intermediate wire capacitances leads to increased gate sizes. Several energy efficient solutions can be derived with a very little loss in delay. The proposed formulation can serve as an upper bound to the designer so as to calculate how much he can stress the design gaining a few more picoseconds.

Fig. 3(a) illustrates the delay of an example path, when stage effort f_2 is independently increased up to 2× its minimal value. For each case, stage effort f_1 is recalculated since the input capacitance of the second chain is gradually reduced. Each line of Fig. 3(a) refers to an input capacitance between 1fF and the maximum allowed, that is 10fF. In all cases when varying f_2 the delay loss is negligible (almost flat lines). The form of the delay plots, proves that a wide variety of stage efforts give delays close to the minimum. This is the reason why simplified solutions to the problem of gate sizing with intermediate interconnect [9]–[10] work well in most practical cases. However, even small differences of the input capacitance used by the path negatively affect the delay. In Fig. 3(b) the normalized sum of the input capacitances of all the gates of the circuit is shown. It is evident that the gain in area and energy can be of more than 20% when increasing f_2 1.5× its minimum value. The corresponding delay loss is less than 4%. From both figures we conclude that significant gains can be achieved when varying the stage effort of the rear paths with almost no delay cost. In contrast it is advantageous to use the maximum allowed input capacitance of the path, since for smaller values the delay rapidly increases without offering significant energy savings.

3.2 Extension to Arbitrary Logic Paths

Real circuits contain several types of logic gates, characterized by different values of logical effort and parasitic delay. Also the gates' output are additionally loaded

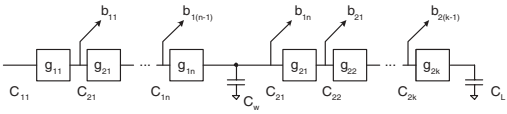


Fig. 4. A general logic path

via branching to other paths of the circuit. All these features of arbitrary logic paths are well handled by the method of logical effort. The delay of a general path with intermediate wire capacitance (see Fig. 4), can be expressed as

$$D = g_{11}b_{11}\frac{C_{12}}{C_{11}} + g_{12}b_{12}\frac{C_{13}}{C_{12}} + \cdots + g_{1n}\frac{C_w + b_{1n}C_{21}}{C_{1n}} + g_{21}b_{21}\frac{C_{22}}{C_{21}} + \cdots + g_{2k}\frac{C_L}{C_{2k}}$$

In order the delay of the path to be minimized, the stage efforts of the first and the second chain of gates should satisfy the following equations.

$$f_1^{n-1}(f_1 - f_2) = G_A \cdot B_A \cdot \frac{C_W}{C_{11}} \quad \text{and} \quad f_1^{n-1} f_2^{k+1} = (G_A \cdot G_B) \cdot (B_A \cdot B_B) \cdot \frac{C_L}{C_{11}} \quad (12)$$

G_A is the product of the logical efforts of the gates of first chain (up to the intermediate wire) and G_B the corresponding logical-effort product of the gates of the second chain (after the wire capacitance). The branching efforts of the two paths B_A and B_B are defined in a similar way. The new equations have the same format as in the case of the two inverter chains (Eq. (3) and (4)). However, the new terms on the right side of both equations contain also the products of the logical and branching effort of each path, which resembles the definition of path effort [2]. The main difference is that when wire capacitance is considered, two separate definitions of the path effort are needed.

The bounds (9)–(11) can also provide the stage efforts f_1 and f_2 in the case of a general logic path by substituting C_L and C_w with their effective equivalents. The effective wire and load capacitances $C_{w,\text{eff}}$ and $C_{L,\text{eff}}$ are defined as

$$C_{w,\text{eff}} = C_w \prod_{i=1}^{n-1}(g_{1i}b_{1i}) \qquad \text{and} \qquad C_{L,\text{eff}} = C_L \prod_{i=1}^{n}(g_{1i}b_{1i}) \prod_{i=1}^{k}(g_{2i}b_{2i}) \qquad (13)$$

It should be noted that $C_{L,\text{eff}}$ contains the product of the logical and the branching efforts of all the gates from the source up to the end of the path, while $C_{w,\text{eff}}$ uses only the gates before the wiring capacitance, excluding the last one. In the general case, in order to compute the input capacitances of the gates, besides the computed stage efforts, the logical and branching effort of each gate should be also taken into account [2].

4 Optimal Number of Stages

Having an accurate and easy-to-use method for deriving the optimal stage efforts, the designer can easily and quickly decide the number of stages n and k that

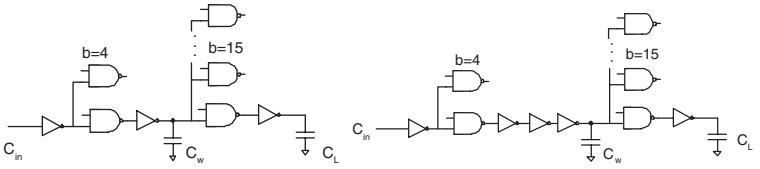


Fig. 5. Selecting the optimal number of stages

are better suited to drive both the wiring and the output load capacitance. It is well known that the best number of stages for the simple chain of gates with no intermediate interconnect capacitance is roughly equal to $\log_4(G \cdot B \cdot C_L/C_{in})$.

When interconnect capacitances are included, it is difficult to derive a simple metric that gives the optimal number of stages. Hence, we propose a simple approach that uses only the derived bounds. Assume for example that $C_{\text{in}} = 5\text{fF}$, $C_w = 300\text{fF}$ and $C_L = 100\text{fF}$. We would like to simply evaluate in terms of delay the two alternatives shown in Fig. 5. For the first case the effective loading and wiring capacitances are equal to $C_{w,\text{eff}} = 300 \times g_{\text{nand}} \times 4$, $C_{L,\text{eff}} = 50 \times g_{\text{nand}}^2 \times (4 \times 15)$, where in our technology $g_{\text{nand}} = 1.18$ and $p_{\text{nand}} = 1.71$. Therefore, using (9)–(11) the expected stage efforts are equal to $f_1 = 7.75$ and $f_2 = 3.03$ and thus the expected minimum delay, including parasitic delays, is 36τ. Following the same procedure for the second case the expected minimum delay is 31.3τ ($f_1 = 3.66$ and $f_2 = 2.1$). Therefore with just a few value substitutions we conclude that the second alternative, i.e., five stages in the first chain, is advantageous and gives a 13% faster design. When dealing with large intermediate wire loads it is better to add more stages before the wire load so as to minimize its effect.

5 Handling Multiple Levels of Interconnect

In cases that more than two logic paths are separated by fixed interconnect capacitances, the optimal stage effort of each path can be computed using a simple repetitive procedure. In practice, no more than three or four stages of considerable intermediate wire capacitances exist before some form of latching occurs to the outputs of the combinational logic. The proposed method aims in closely approximating the required stage effort of the first chain of gates and then recursively compute the efforts of the remaining gates so as delay to be minimized. Consider for example the path shown in Fig 6. Differentiating the delay of the path with respect to the input capacitances of the gates we get that

$$f_1\,(f_1 - f_2) = \frac{C_A}{C_{\text{in}}}, \quad f_1 f_2\,(f_2 - f_3) = \frac{C_B}{C_{\text{in}}}, \text{ and } \quad f_1 f_2 f_3^2 = \frac{C_L}{C_{\text{in}}}. \tag{14}$$

Solving exactly the three non-linear equations gives that the minimum delay equals to $(12.45 + 3p_{inv})\tau$ and the optimal stage efforts f_1, f_2, and f_3 are equal to 4.63, 2.47, and 0.72, respectively.

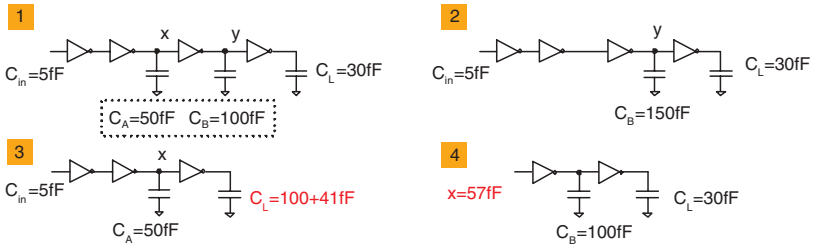


Fig. 6. Steps of the recursive procedure that handles multiple levels of intermediate interconnect

At first, we make the simplifying assumption that $f_1 = f_2$. The assumption that the gates of the first and the second chain have the same effort can be satisfied in two ways. The first one is to ignore the first wiring stage, i.e, C_A is zero [10]. As shown in Section 3, this approach clearly underestimates the input capacitance of the gates closer to the end of the path. In the proposed method we choose an alternative approach. Adding the two first equations of (14) and setting stage effort f_1 equal to f_2 it is derived that $f_1^2(f_1 - f_3) = (C_A + C_B)/w_1$ and $f_1^2 f_3^2 = C_L/w_1$. The new equations can be translated to the equivalent circuit shown in step 2 of Fig. 6, where the effect of the first wire is added to the next level. The resulting path can be easily sized following the procedure described in Section 3. Computing the bounds of f_1 and f_3 it is derived that for minimum delay the input capacitance of the last stage should be $y = 41$fF.

Since we have one first approximation of the input capacitance of the last stage we continue with step 3, where the loading capacitance is replaced by the combined effect of C_B and the value derived in the first step. Substituting the new parameters to (9)–(11) we get that the input capacitance of the second chain x should be equal to 57fF and the stage effort of the first chain is $f_1 = 4.628$.

At this point we assume that the stage effort of the first chain has been correctly approximated. In fact this is true in our example. Although this seems a rough estimate, it is a valid assumption. According to the form of equations (14) when increasing the stage effort of a chain closer to the input, the following chains immediately require a smaller stage effort. In this way, when one chain gets a near optimal value all the other stage efforts are simultaneously bounded closer to their minimum values too. Continuing with our example, after fixing the input capacitance of the second chain to 57fF, the remaining path needs to be sized (step 4). The resulting stage efforts f_2 and f_3 are equal to 2.48 and 0.725 while the new input capacitance of the last chain equals $y = 41.3$fF. Since the initial approximation of $y \sim 41$fF is roughly equal to the final value, the procedure stops since all stage efforts have converged closely to their minimum values. It can be verified that the computed stage efforts are almost exact.

We have experimentally verified for 1000 randomly generated paths that only one iteration suffices to predict the minimum delay of the circuit with no more than 2% error. If the initial and the final approximation differ significantly one more backward iteration is required to get the exact value. The new iteration

should start with step 3, where the output load is increased by the new estimated capacitance. In cases of more intermediate interconnect levels the recursive procedure works exactly the same way. In each step all preceding wiring capacitances are added to the wiring capacitance closer to the output and new estimates are computed until the stage effort of the first path converges to its optimal value.

6 Conclusions

A simple and accurate method for performing gate sizing with intermediate fixed wire capacitances has been presented in this paper. Wiring characteristics are predominant in very-deep submicron technologies, and their effects need to be analyzed and solved early in the design cycle. Therefore, the designer can truly benefit by the adoption of the proposed approach. The development of a practical framework that would treat in a unified manner both wire resistance and capacitance during gate sizing is a subject of ongoing research.

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